

LISA Phasemeter prototyping

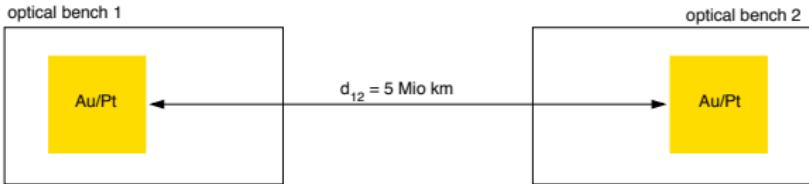
Vinzenz Wand, Gerhard Heinzel and Karsten Danzmann

Albert-Einstein-Institut Hannover, Max Planck Institute for gravitational physics and University Hannover

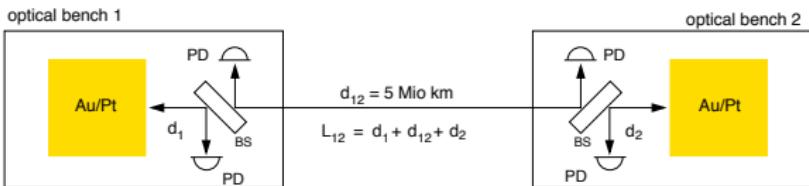
LISA Symposium 6, 23rd June 06



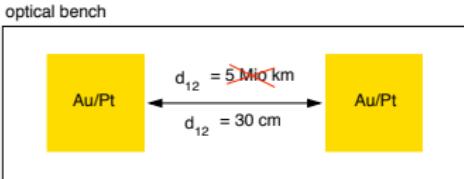
proof mass - proof mass measurement



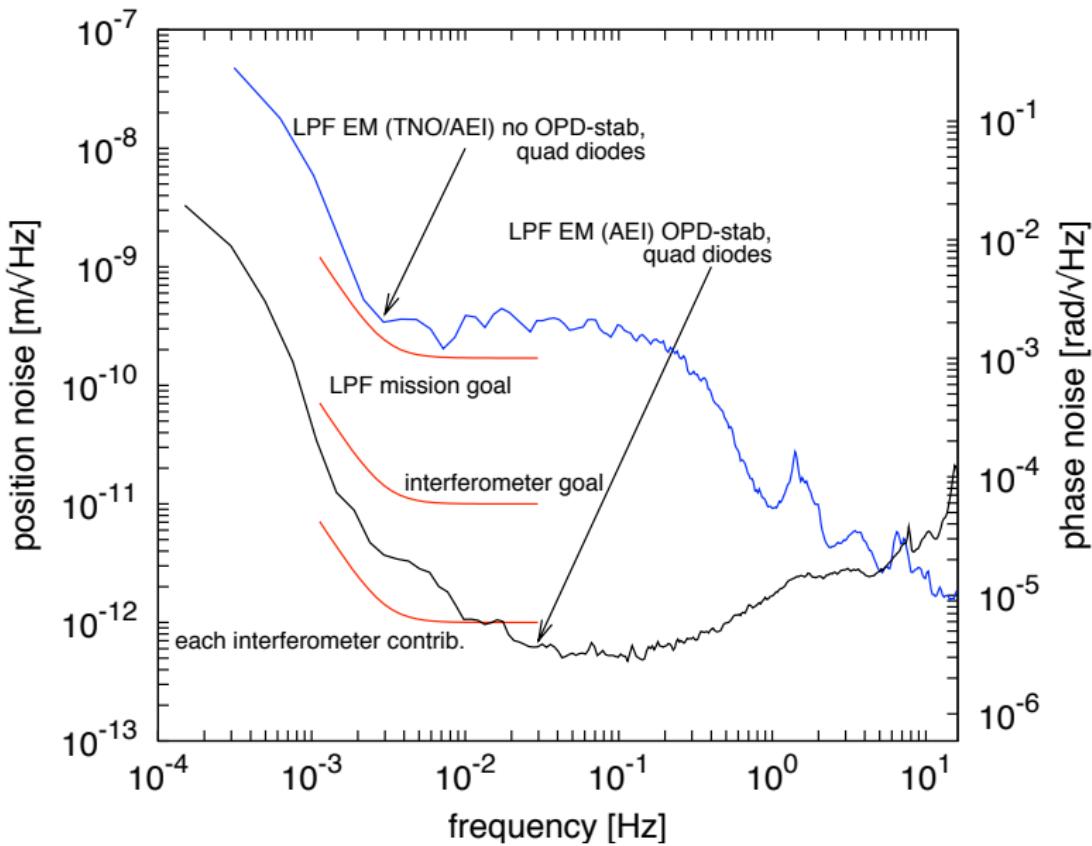
splitted interferometry



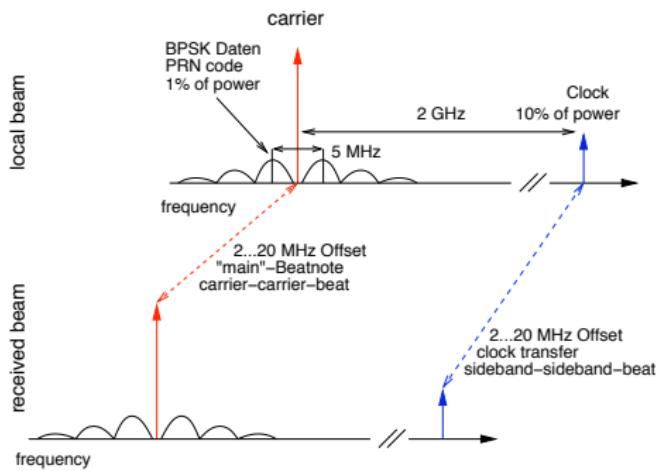
LISA Pathfinder



LISA pathfinder phase measurement performance



LISA phase measurement

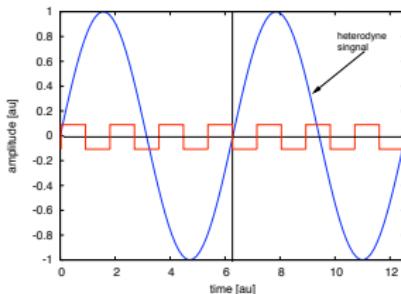


proposed modulation scheme:

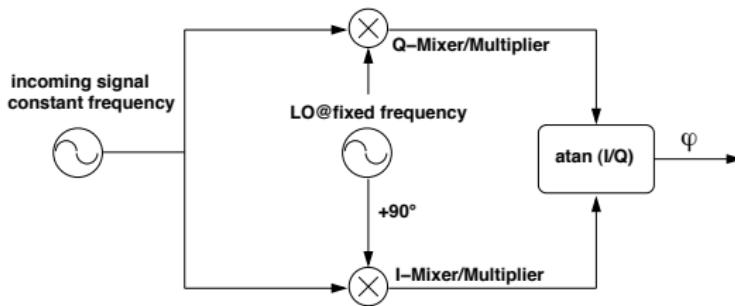
- phase measurement of carrier-carrier-beats wrt. local clock provides main science measurement
- clock transfer by sideband-sideband beat
 - 2 GHz sideband frequency but sb-sb-beat at appr. same frequ. as carrier-carrier beat
- data transfer and ranging measurement (GPS-like) via Pseudo-Random-Noise-Code (PRN)



- **zero crossing technique** counting fast clock cycles between signal zero crossings: has been demonstrated for LISA Pathfinder

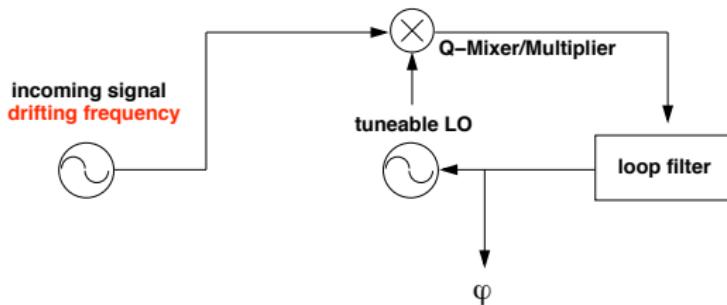


- **(SB)-DFT based phasemeasurement:** implemented in LISA Pathfinder



- **Phase locked loop measurement**

similar to the SBDFT readout but the local oscillator tracks via a PLL the drifting carrier frequency

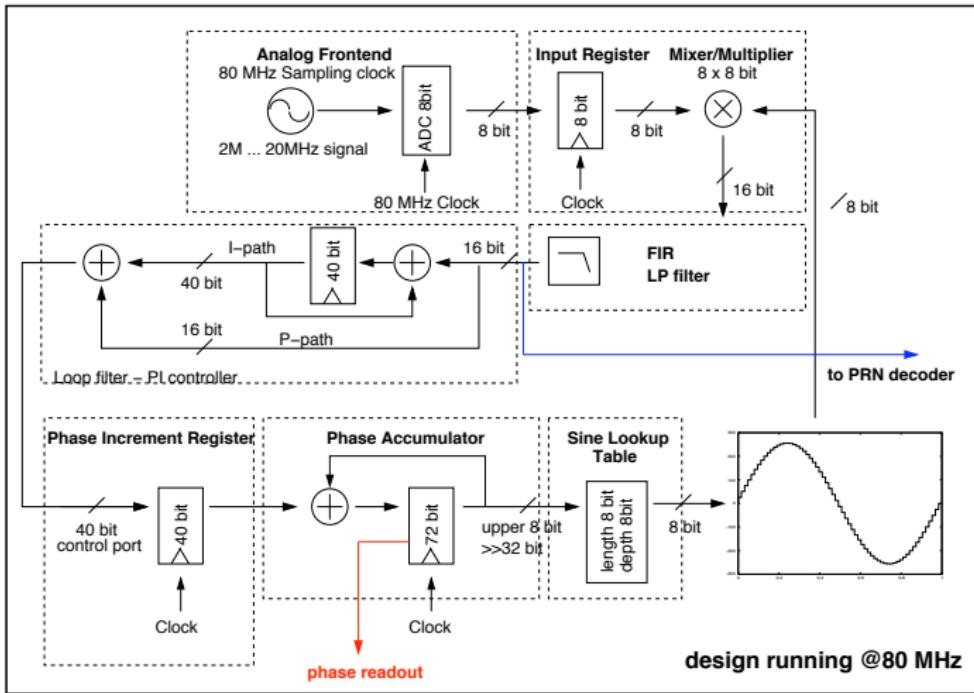


phase information obtained by e.g. feedback readout

Allocated PMS noise is $1 \text{ pm} / \sqrt{\text{Hz}} \approx 6 \mu\text{rad} / \sqrt{\text{Hz}}$.



The ADPLL approach



- digital PLL tracks carrier beat
- rapid sampling of beat signal at appr. 80 MHz
- phase measurement: of phase increment register (PIR) or phase accumulator (PA) readout
- error signal outside the control bandwidth will be used for PRN Demodulator



- incoming beat note between 2 MHz and 20 MHz
->caused by Doppler drift induced frequency variation of max. 4 Hz/s
- direct sampling with 8 bit AD converter running at 80 MHz,
- its digitisation noise is $\delta\tilde{\varphi} = 2.84 \times 10^{-8} \frac{\text{rad}}{\sqrt{\text{Hz}}}$



Phase detector

- The NCO output signal has to be phase locked to the incoming signal.
Therefore a 8x8 bit multiplier acts as a mixer for the two signals.

DDS

- A 72 bit accumulator with a 40 bit phaseincrementregister is the core of the a Numerically controlled oscillator (NCO).
- The upper 8 bit of the accumulator are connected to a 256 element sinetable with a resolution with 8 bit.
- 80 MHz Clock drives the NCO. For a synthesised signal the resulting digitisation noise of the output signal of the NCO is given by

$$\delta\tilde{\varphi} = \frac{2^{-B}}{2 \cdot \pi \cdot \sqrt{6 \times f_{\text{sampl}}}} \cdot \frac{\text{rad}}{\sqrt{\text{Hz}}} \quad (1)$$

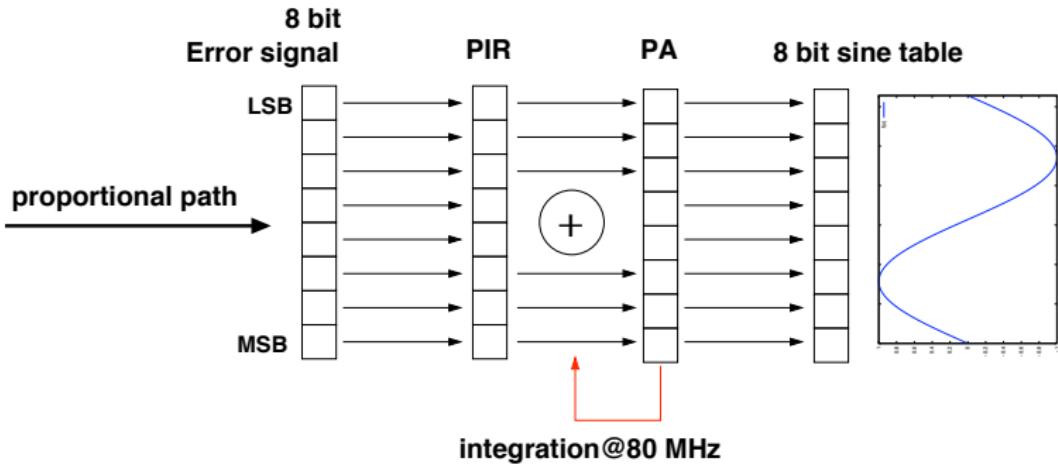
(where B is the effectiv number of bits)

- resulting phase error $\delta\tilde{\varphi} = 2.84 \times 10^{-8} \frac{\text{rad}}{\sqrt{\text{Hz}}}$

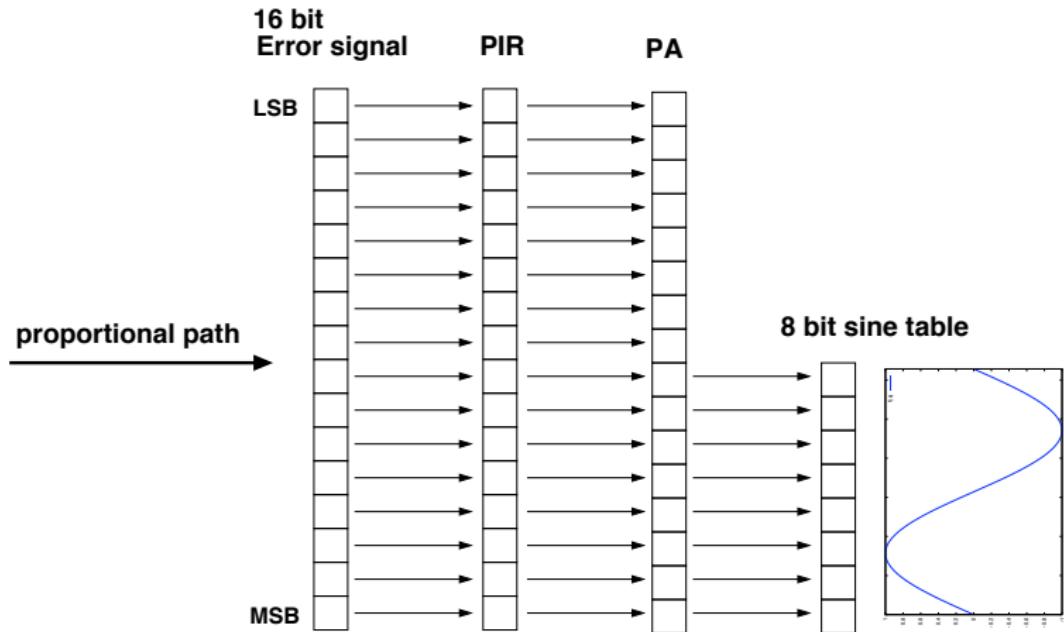


The DDS System - frequency generation

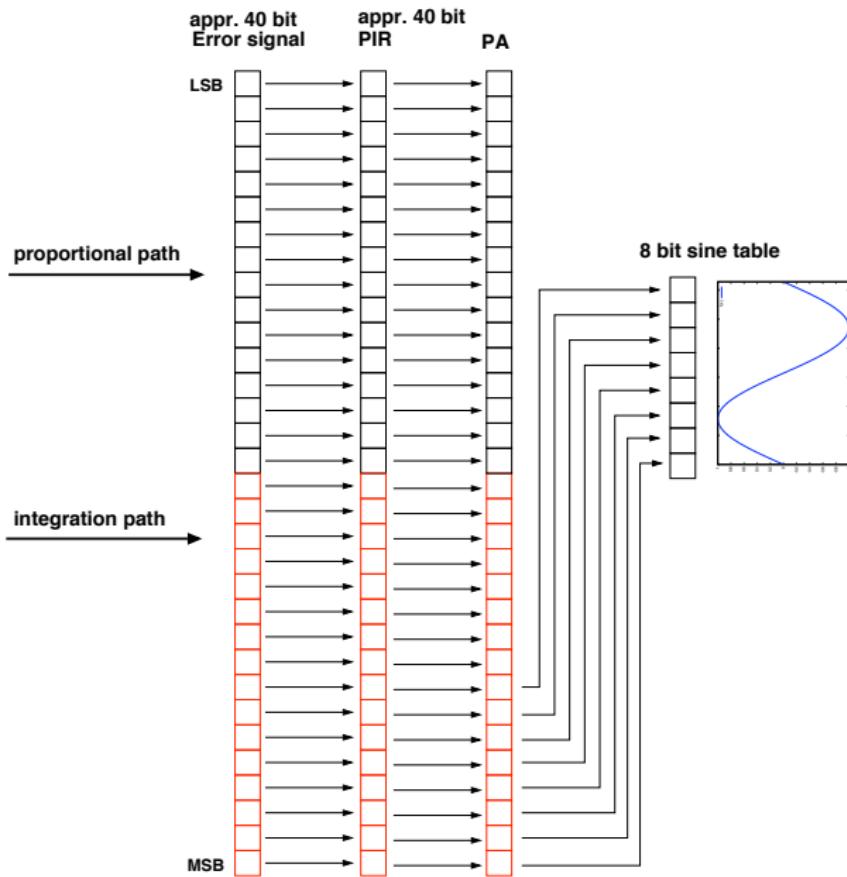
80 MHz sampling rate in combination with a 8 bit sine table leads to a DDS base frequency of $f_{\text{base}} = \frac{80 \cdot 10^6 \text{ MHz}}{2^8} = 312500 \text{ Hz}$.



- obtaining higher frequency resolution:

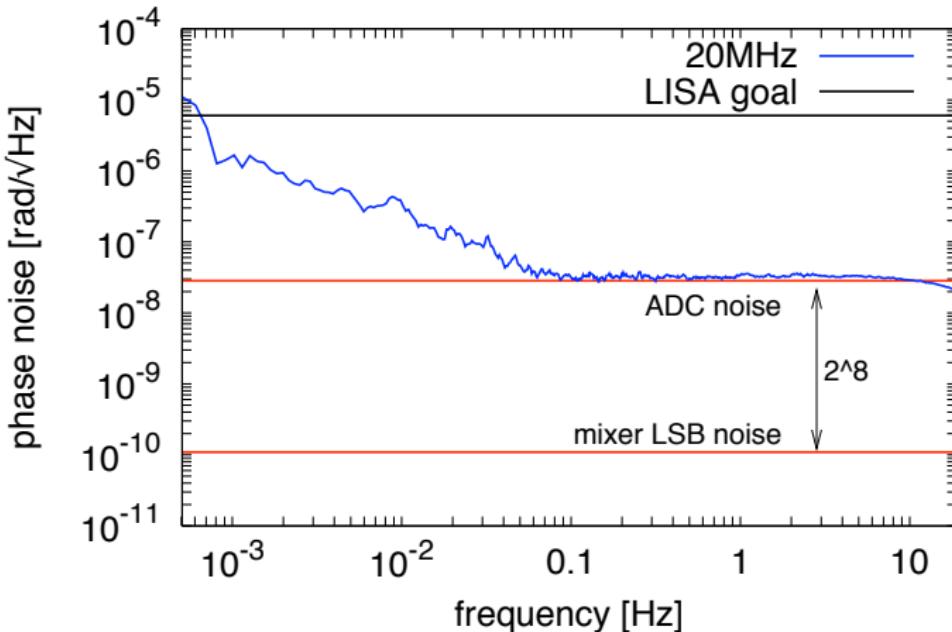


The DDS System - frequency generation



preliminary

phase meter performance 20MHz
starting with 5 kHz offset

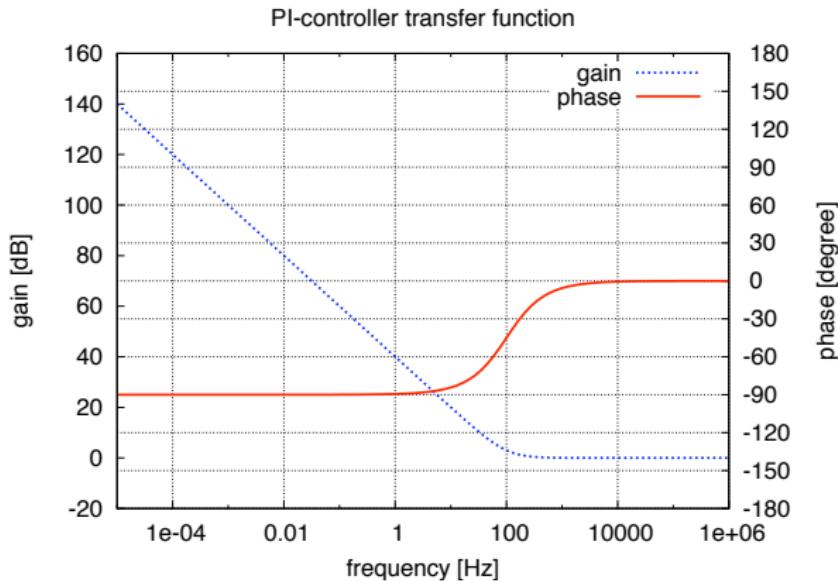


Loop filter transfer function

The loop filter has been implemented as a proportional integration controller (PI-controller) with the transfer function:

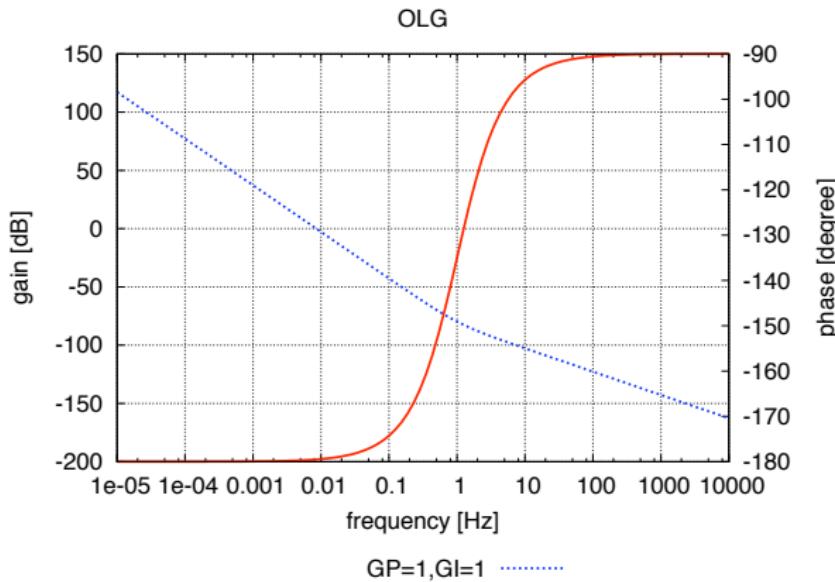
$$G_F(\omega) = G_p + \frac{G_i}{i\omega} \quad (2)$$

with a cutoff frequency of $f_c = \frac{G_i}{G_p}$.



Loop filter transfer function

The only free parameters left are G_P which determines the overall gain factor and G_I where the ratio $\frac{G_I}{G_P}$ determines the crossover frequency between the $1/f$ and the $1/f^2$ range. The OLG of the system for $G_I = G_P = 1$ can be seen in the following picture.

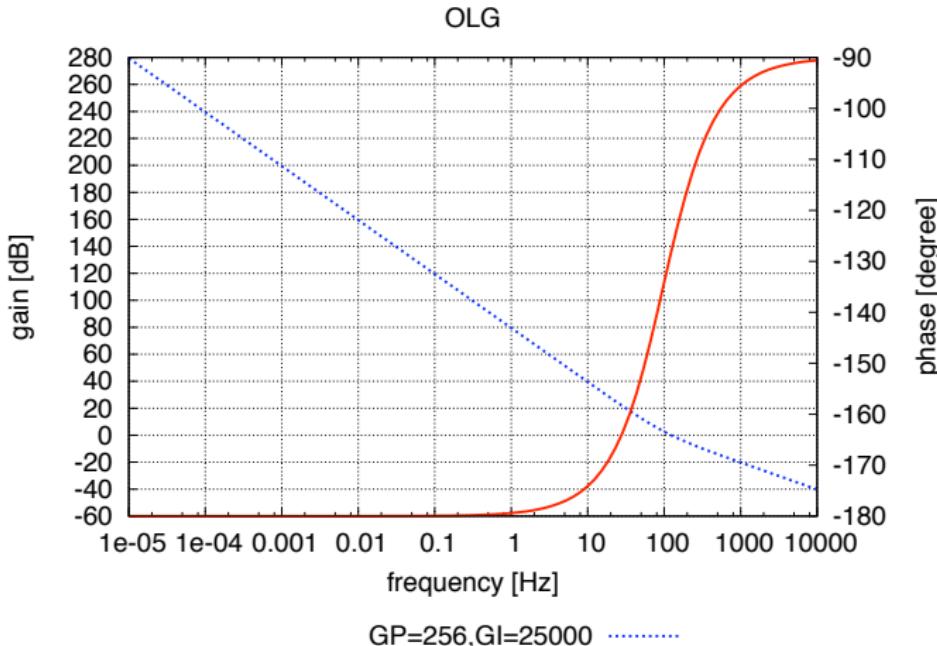


This loop is not stable



Loop filter transfer function

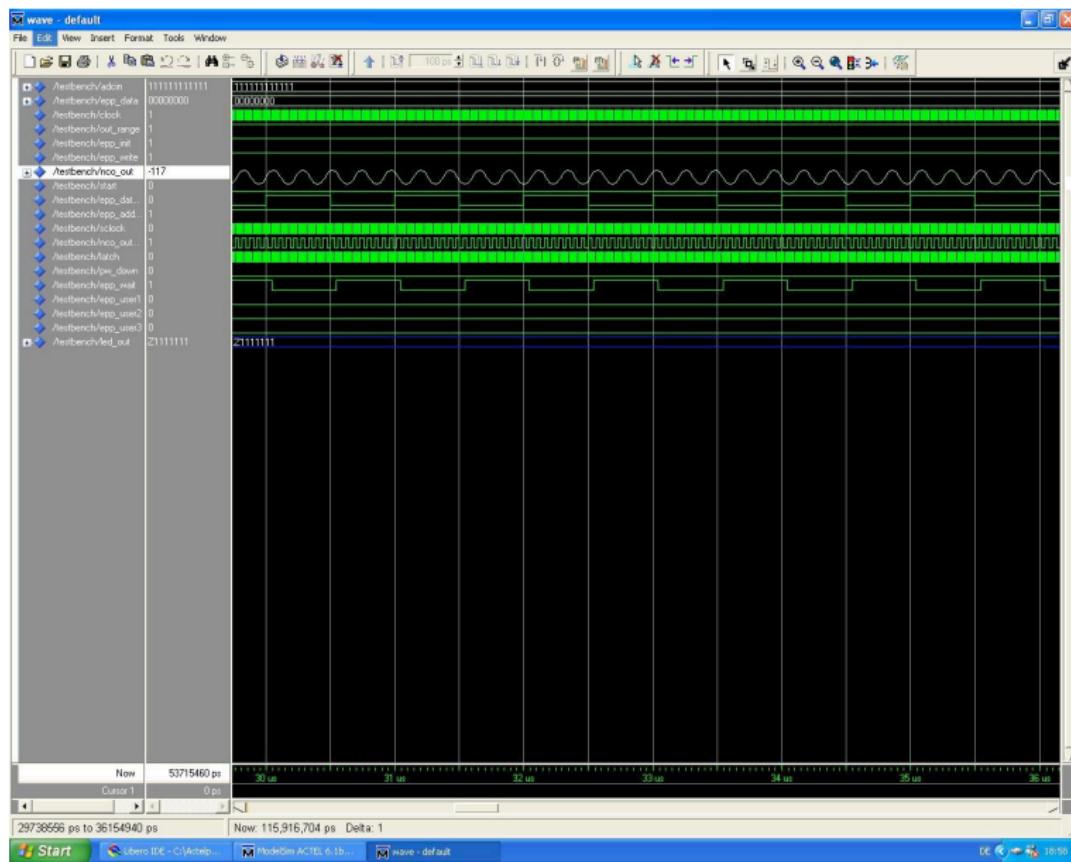
The following graph shows the configuration for $G_P = 256, G_I = 25000$.



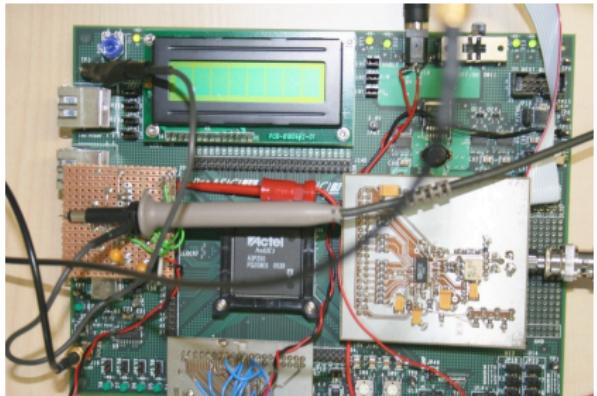
Note: A proportional Gain larger than "1" leads to losses in the sensitivity of the frequency tuning.



VHDL Development tool (ModelSim)



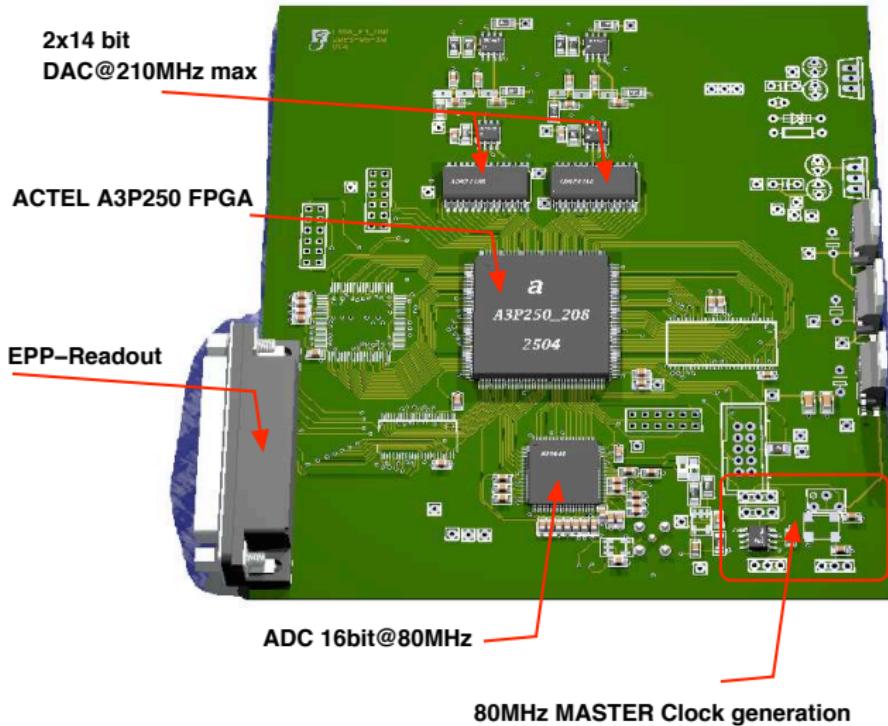
Hardware implementation



- implementation of phasemeter on an Actel FPGA (Field Programmable Gate Array)
- programming via VHDL (Very High Speed Integrated Circuit Hardware Description Language)
- phase readout of the phase accumulator via EPP Port



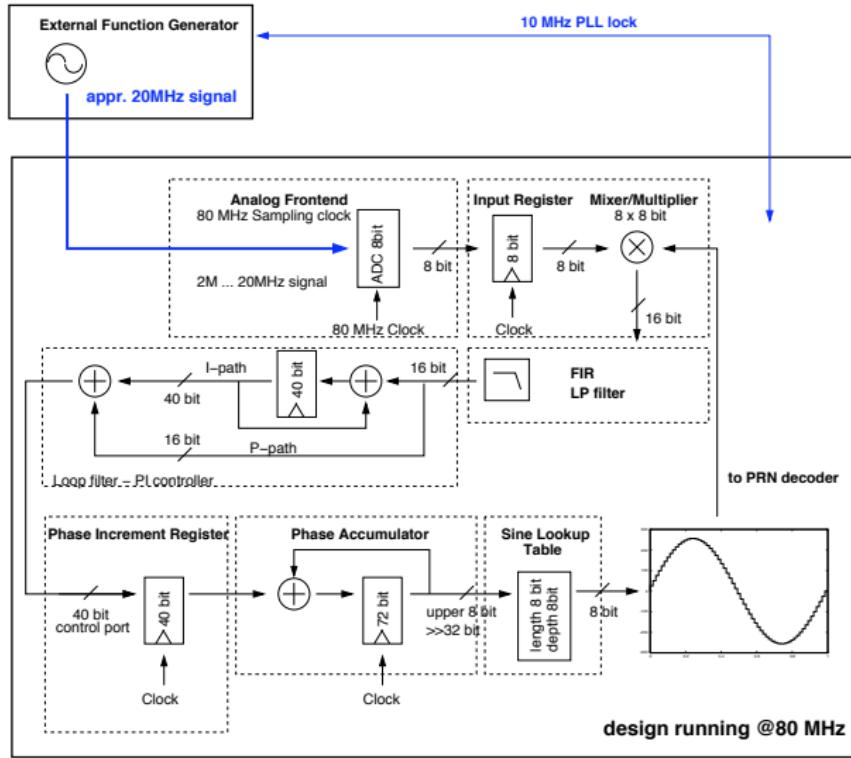
Hardware implementation

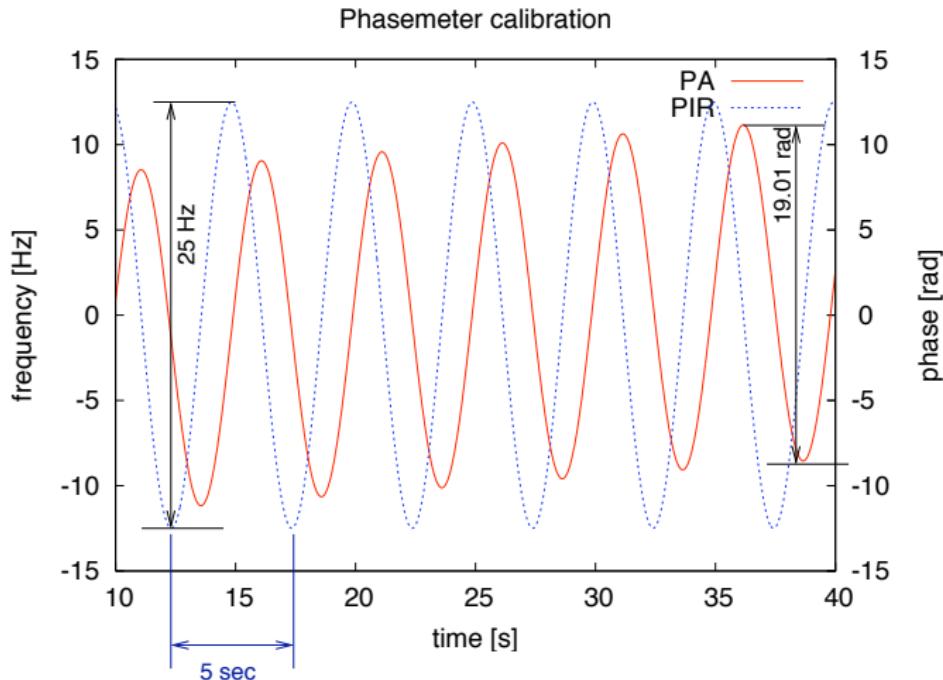


- CAD of new board design
- estimated delivery date: end of June 2006
- same FPGA type as the prototype board - no VHDL design changes necessary



test setup1

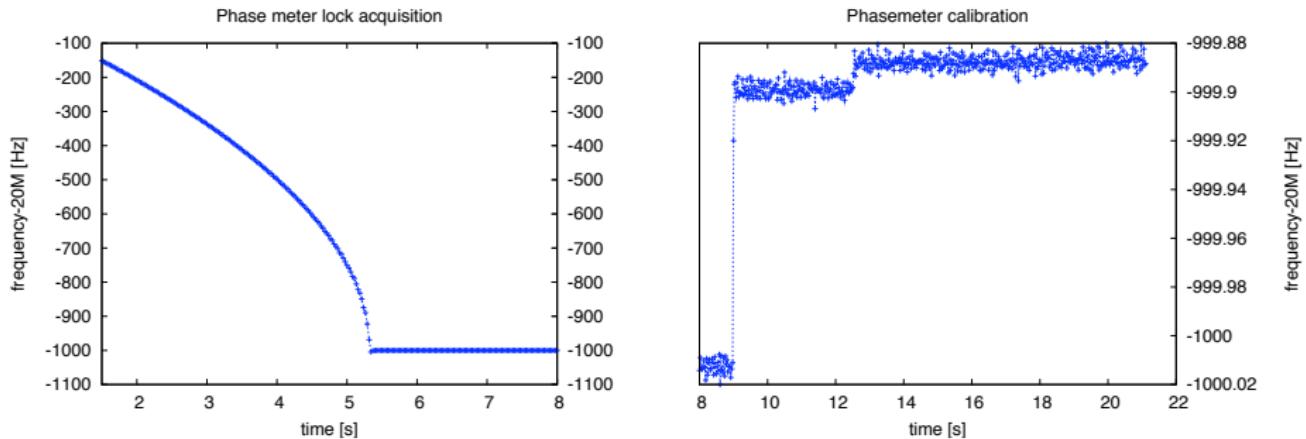




- Reference Signal 19.999 MHz, frequency modulated:
 $f_{\text{mod}} = 200 \text{ mHz}$, $\Delta f = 12.5 \text{ Hz}$



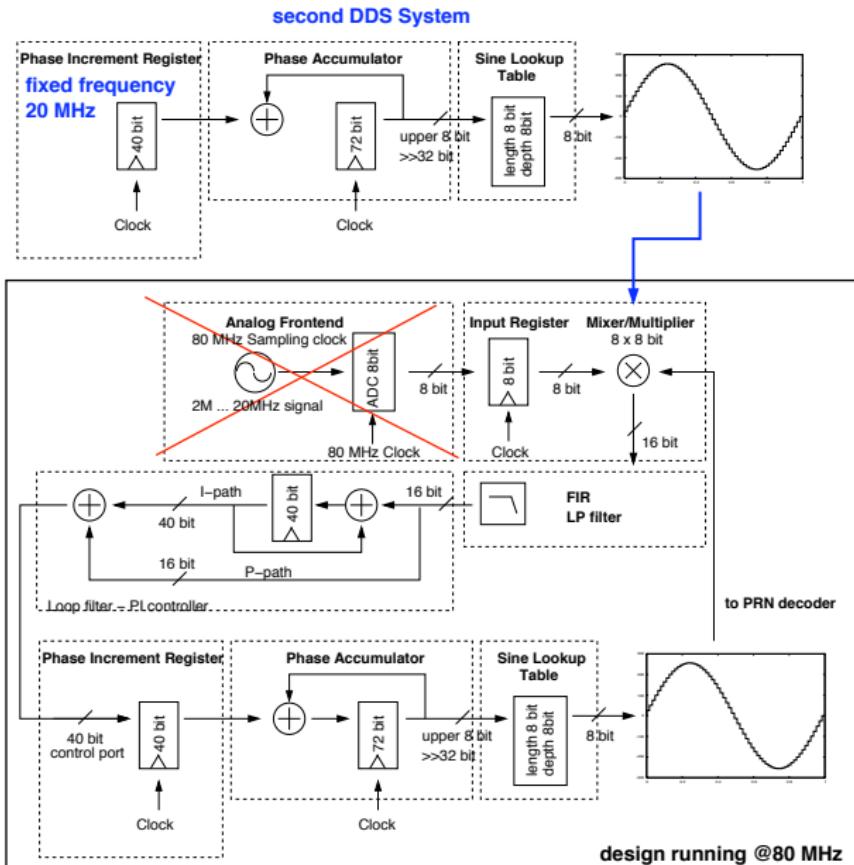
Lock Acquisition



- left graph shows PM lock acquisition to an external 20 MHz signal, sampled by ADC, starting with a 1 kHz offset
- right graph shows 100 mHz and 10 mHz calibration step

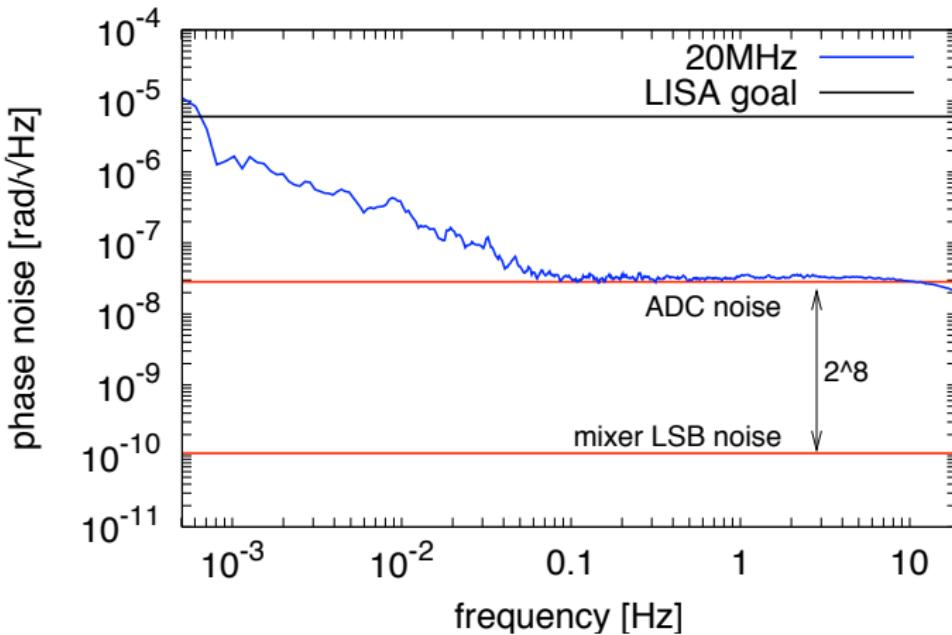


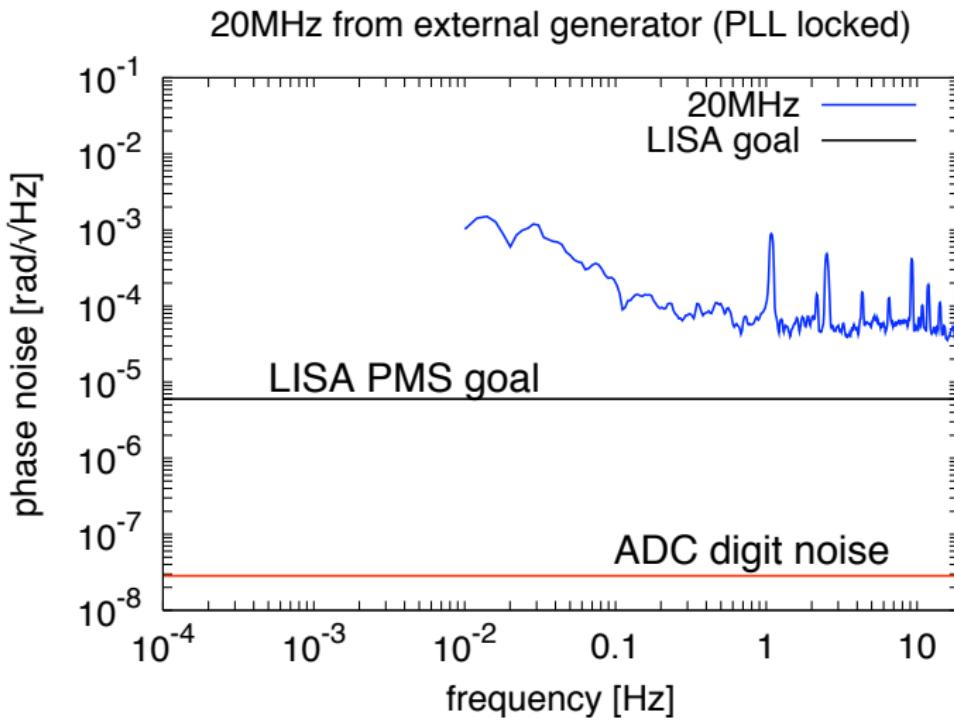
noise performance (test setup2)



preliminary

phase meter performance 20MHz
starting with 5 kHz offset





Conclusion

- LISA - prototype phasemeter has been developed
- system provides core functionality for main science data readout (phase readout and carrier tracking)
- design parameters are sufficient for required noise performance
- system meets requirement with synthetic signals

Outlook

- ongoing system improvement (noise investigation)
- testing the system with optical setup
- an improved hardware design is in implementation
- implementation of data transfer / ranging functionality

